Scuola universitaria professionale della Svizzera Italiana
Dipartimento tecnologie innovative

SUPSI

Edge AI on ultra-low-power embedded platforms

Modulo breve

Presentazione

Artificial intelligence (AI) combined with the ultra-low-power (ULP) paradigm is fueling the rapid evolution of embedded domains, such as Internet-of-Things and Industry 5.0.
In this context, the RISC-V instruction set architecture is leveraging significant momentum, rising among top-notch industrial players: Google, IBM, Intel, Qualcomm, and even Nvidia use RISC-V in their chips now.
This course will introduce the attendees to a RISC-V-based multi-core ULP processor. We will provide theoretical foundations and hands-on experience to optimize and deploy AI applications at the extreme edge.

Obiettivi

This class aims at people with some background in embedded programming who are eager to learn novel, cutting-edge technologies which leverage the RISC-V architecture for Artificial Intelligence (AI) workloads.
We will offer the attendees the possibility to challenge their skills and endorse their know-how with a practical course that frames theoretical lectures with hands-on sessions.

Destinatari

Our ideal candidate has a basic knowledge of the embedded systems field and is willing to expand their expertise to the latest cutting-edge technologies from the RISC-V-based ultra-low-power domain.

Requisiti

- Familiarity with embedded devices (e.g., STM32 MCU, TI MSP430 MCU);
- Familiarity with C programming (e.g., flow control, functions, arrays, pointers).
- Familiarity with Linux OS (e.g., Ubuntu).
- Favorable basic parallel programming experience (e.g., CUDA).

Certificato

Certificate of attendance

Programma

1. Introduction to the GWT GAP8 parallel ultra-low-power SoC
- Basic concepts of embedded devices
- SoC's architecture overview (programmer's point of view)
- SDK, tools, virtual platform, and quick-start [hands-on application]

2. Memory hierarchy and data locality
- L1 (TCDM), L2 shared memory, off-chip memories, and instruction cash
- Direct memory access (DMA), scratchpad, double-buffering techniques
- Optimized memory orchestration and profiling [hands-on application]

3. Multi-core parallel programming
- Single instruction multiple data (SIMD) paradigm
- From sequential to parallel programming
- Basic linear algebra kernel parallel implementation [hands-on application]

4. AI-based application at the edge
- Basic deep learning concepts
- Convolutional neural networks: basic operators
- Parallelization of a complete AI-based workload [hands-on application]

Durata

12 hours-lecture

Responsabile/i

Roberto Mastropietro, Professor at SUPSI

Relatore/i

Daniele Palossi, Postdoctoral Researcher at the Integrated Systems Laboratory (IIS) of ETH Zurich and at the Dalle Molle Institute for Artificial Intelligence (IDSIA), USI-SUPSI.

Date

January 25, February 1, 8, 15, 2023

Orari

17.30-20.00

Luogo

SUPSI, Department of innovative technologies, Polo universitario Lugano - Campus Est, Via La Santa 1, 6962 Lugano-Viganello
Lectures will be offered in a hybrid format, where candidates can attend either in taught class or online (e.g., Zoom).

Costo

CHF 450.00
There is a 10% discount for individual members of AFTI, AITI, ATED e itSMF

Osservazioni

Language selection criteria:
At the registration time, each candidate will send an e-mail to dti.fc@supsi.ch indicating their preferred language among:
. Italian only;
. English only;
. no preference -- i.e., meaning both Italian and English are fine.
Once the registrations are closed, the language with the higher preference will be selected as the final class's language. Then, the candidates will have to finalize their registration, i.e., implicitly allowing for free withdrawal in case of an unsuitable course's language.

Contatti

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Informazioni

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Termine d'iscrizione

December 23, 2022

Link per le iscrizioni

https://fc-catalogo.app.supsi.ch/Course/Details/36913